Improving Operational Stability of p-Type Field-Effect Transistors by Charge Selective Electrodes: a General Strategy

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Operational instability caused by unintentional electron injection is a common problem for field-effect transistors (FETs) based on relatively narrow-bandgap semiconductors. Typically, the electron injection is followed by electron trapping at the semiconductor/dielectric interface or sometimes in the bulk semiconductor, resulting in a modification of the built-in field in the FETs. Such a dynamic process causes continuous threshold voltage or Dirac voltage ($V_{th/Dirac}$) shift and thus unstable device operation. A charge-selective electrode (CSE) design is used to address these problems. The CSE is formed by inserting a molybdenum trioxide interlayer between the electrode and the semiconductor, which creates an energy barrier to block electron injection. It is shown that the CSE strategy can generally work for FETs based on three semiconductor families, namely conjugated polymer, graphene, and quantum dot, and greatly suppresses the $V_{th/Dirac}$ shift, enhancing the bias stress stability as well as reducing the noise level of the FETs. The mechanism for CSE-reduced bias stress is investigated through trap analysis. CSE is a general strategy for achieving stable and low-noise operation of unipolar FETs. The device design concept can be applied to other device configurations.

1. Introduction

Field-effect transistors (FETs) based on narrow bandgap semi-conductors, such as organic molecules,[1–4] colloidal quantum dots (QDs),[5,6] and 2D materials (e.g., graphene),[7–10] have been extensively researched for applications in large-area or flexible circuits, near-to-mid infrared photodetectors and chemical- and biosensors, as they provide advantages including

low-temperature processability, mechanical flexibility, and tunable electronic properties.[8,9,11–15] The performance of the FETs has been greatly improved in recent years owing to the rapid enhancement of the field-effect mobility of the semiconductors and the improved quality of the semiconductor/dielectric and semiconductor/electrode interfaces. However, the operational stability of FETs is still unsatisfactory for many practical applications where extensive bias stress results in an unstable device current or voltage output. For example, when an organic FET (OFET) is used as a photodetector to monitor human's arterial pulse signals, its large direct-current (DC) drift prevents the device from tracking the DC component of the signal, resulting in loss of the critical information regarding blood flow.[16] For graphene FETs (GFETs), bias stress with a positive Dirac voltage shift was reported in both single- and multilayer- graphene-based devices and also led to operational instability.[17] Bias-stress could be particularly severe for QD based FETs (QD FETs). For instance, during the current–voltage (I–V) scans of some lead sulfide (PbS) QD FETs the source-drain current dropped so rapidly during voltage sweep that it is even difficult to accurately extract device parameters such as mobility and threshold voltage from the I–V curves.[18]

The bias-stress effect is associated with the threshold voltage (V_{th}) or Dirac voltage (V_{Dirac}) shift when an FET is continuously turned on.[19] Fundamentally, this is often associated with charge trapping at the existing or newly generated defect states in the device. Methods of reducing structural or interface defects in FETs have been reported to improve the bias-stress stability significantly. For instance, Nikolka et al. introduced molecular additives to the semiconductor layer of OFETs; these molecules can displace water from the voids in the semiconductor and subsequently eliminate water-induced traps, thus greatly enhancing the ambient stability of the devices.[20,21] Liu et al. applied atomic layer deposition to infill the lead selenide (PbSe) QD layer of an FET with amorphous alumina and show the process could effectively passivate the QD surface states and increase the operational stability.[22] A similar passivation method has also been proven to increase the stability of GFETs.[23]

For GFETs and narrow-bandgap OFETs and QD FETs, electron-trapping at the semiconductor/dielectric interface often results in electrical instability as the trapped electrons could

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modify the built-in field of the FETs and thus shift the threshold voltage.[24] Self-assembly monolayer (SAM) is often used to passivate the surface defects of the commonly used dielectric oxide (e.g., SiO_2) and the treatment has been applied to FETs based on organic materials,[25] graphene[26] and QDs.[27] Besides defect passivation, a trap competing mechanism has been proposed to address the electrical instability problem.[28] In this method electron acceptors such as [6,6]-phenyl-C61-butyric acid methyl ester ($PC_{61}BM$) are used to out-compete SiO_2 in electron trapping in a p-type OFET; as a result, the electron trapping are largely reduced at the dielectric/semiconductor interface, where the concentration of holes is the highest, and the stability of the FET is largely enhanced. Alternatively, reduction of surface electron trapping can also be realized via low-defect dielectric, such as Cytop for OFET[29] and GFET.[30] It can be noted that the aforementioned studies attempt to address the instability issue by removing or competing with the interface electron traps. However, since the traps cannot be completely removed, for prolonged operation electron trapping may still occur and cause instability in long-term.

In this work, we propose to introduce a charge-selective electrode (CSE) method that could be used in combination with the trap removing or trap competing approaches to suppress the bias stress behaviour of FETs, and we demonstrate that the CSE approach may be applied generally to narrow-bandgap organic semiconductors, QDs and 2D materials such as graphene. Specifically, we focus on p-type FETs and use molybdenum oxide (MoO_{3-x}) modified gold as the CSE to block electron injection into the semiconductor layer, thus eliminating or suppressing electron trapping in the bulk semiconductor or at the semiconductor/dielectric interface. MoO_{3-x} is nontoxic, stable in air and can be easily deposited via thermal evaporation. It has widely been used as an electrode modification layer to facilitate hole-injection and electron-blocking in organic photovoltaic cells (OPVs),[31] organic light emitting diodes (OLEDs),[32] and silicon solar cells,[33,34] but its application in transistor structures has not been well explored. MoO_{3-x} was also reported to improve the source-drain contact of OFETs, and thereby their operational stability, but the effect is mainly for planar and short-channel device configurations.[35–37] Here we incorporate MoO_{3-x} modified CSEs in OFETs, QD FETs, and GFETs, respectively and show that all devices exhibit reduced $V_{th/Dirac}$ shift and greatly improved DC stability under bias stress as a result of suppressed electron injection. Moreover, the low-frequency noise current of the devices is significantly reduced, which is critical for sensing applications. To further elucidate the correlations among bias stress, electron trapping, and hole trapping, we analysed the bias-stress dynamics at different operation conditions. The results suggest that electron trapping-induced hole trapping mainly accounts for the fast decay component of a bias stress process.

2. Material Selection and Working Mechanism

To confirm the generality of the CSE, we chose three kinds of narrow (zero) bandgap p-type semiconductors to make the testing FET devices, which include a donor-acceptor copolymer poly[2,5-(2-octyldodecyl)-3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno[3,2-b]thiophene)] (DPP-DTT),[38] graphene,[39] and PbS QD.[40] To simplify the fabrication process, we adopt a top-contact, bottom-gate FET structure using a heavily doped silicon wafer as the gate electrode and its thermal oxide (≈300 nm thick SiO_2) as the dielectric layer. A SAM treatment with octyltrichlorosilane (OTS-8) is applied to the SiO_2 to reduce its surface trap states for OFETs. Gold (Au) and MoO_{3-x} are patterned on top of the semiconductor layer to form the source-drain electrodes.

The energy diagrams of Au, MoO_{3-x} and the three semiconductors, DPP-DTT, PbS QD, and graphene (in air) are depicted in the left panel of **Figure 1**a.[38–42] It can be seen that MoO_{3-x} can behave like an electron sink to take up electrons when forming contact with Au and the semiconductor; as a result, the energy level of MoO_{3-x} is lifted up relative to its neighbours, forming an energy barrier for electron injection (right panel of Figure 1a; Such energy level arrangement can also be visualized via a Kelvin probe force microscope measurement on the Au/MoO_{3-x}/graphene contact, as shown in Figure S1, Supporting Information). In contrast, in a direct Au-semiconductor contact the electron injection barrier relies only on the work function difference of the two materials, and in many cases, there are surface dipoles at the contact and tail states due to disorder to decrease the electron injection barrier.[43–45]

Figure 1b illustrates the charge injection and transport processes in p-type FETs with unmodified (left), and MoO_{3-x} modified electrodes (right). For the FETs with the unmodified electrodes, electrons can be injected from the drain electrode if the electric field between the gate and drain electrodes overcomes the work function difference at the Au/semiconductor contact; a large portion of the injected electrons will be trapped in the structural and interface defeats, leading to build-up of negative space charges and then a continuous V_{th} shift of the FET. On the other hand, the FET with MoO_{3-x} modified electrode imposes a much larger barrier for electron injection and therefore eliminate or reduce the possibility of electron trapping and accumulation in the device, which is expected to suppress the V_{th} shift and greatly improve the device operational stability.

3. Current–Voltage Characteristics and Bias Stress Effect

To validate the MoO_{3-x} modification effect on the V_{th} (or V_{Dirac}) shift, we measured the transfer characteristics of the modified and unmodified devices by keeping a constant negative drain-source voltage (V_{ds}) while scanning the gate-source voltage (V_{gs}) from different positive values to a constant negative value,[46] as represented in **Figure 2**. Here the electron injection is controlled by gate-drain voltage (V_{gd}), i.e., the larger the V_{gs} (and therefore the V_{gd}) the more electrons injected. It can be seen from Figure 2 that the MoO_{3-x} modification introduces a great difference in the behaviour of V_{th} (or V_{Dirac}) shift under different voltage scans. For the FETs with the unmodified electrodes, the V_{th} (or V_{Dirac}) is shifted with the starting point of the V_{gs} scan. This confirms that increasing the positive V_{gd} indeed induces more electron injection, which then results in electron trapping and threshold voltage shift. In contrast, the transfer curves of the FETs with the MoO_{3-x} modified electrodes remain almost
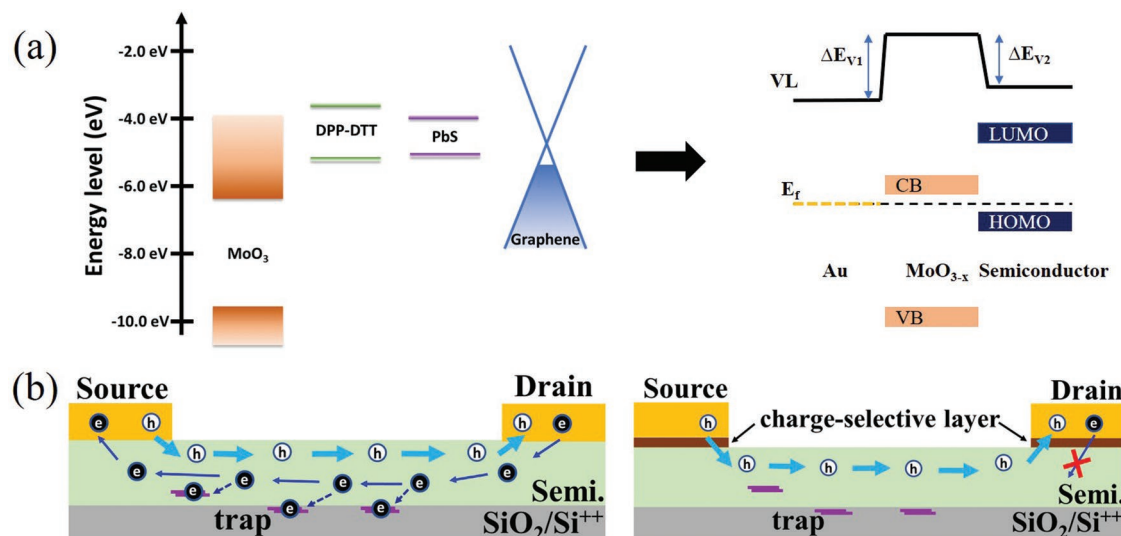
Figure 1. Working mechanism of CSE. a) Left (energy levels before forming contact): Fermi energy level of Au (E_F −5.1 eV), valance band (VB), and conduction band (CB) edges of MoO$_{3−x}$ (VB: −9.7 eV, CB: −6.7 eV), and highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) levels of DPP-DTT (HUMO: −5.3 eV, LUMO: −3.7 eV), PbS QD (VB: −4.0 eV, CB: −5.0 eV), and graphene (E_F: −4.8 eV). The energy level values are adopted from refs. [38–42]. Right: a general schematic diagram illustrating the energy level alignment after forming a contact. ΔE_{v1} and ΔE_{v2} are the energy differences between the vacuum levels of the two contacting materials. b) Schematic diagram of charge injection and transport in the FETs with unmodified Au electrode (left) and MoO$_{3−x}$ modified CSE (right), respectively.

unchanged at different V_{gs} scans, suggesting effective blocking of electron injection. We also note that electron injection could cause some nonideal transfer behavior of OFETs,[28] e.g., the $|I_{ds}|^{1/2}$–V_{gs} curves exhibiting dual slopes (Figure S2a, Supporting Information), and that such behavior is eliminated (for OFETs) or reduced (for QD FETs, Figure S2b, Supporting Information) after the use of the CSE.

After confirming the role of MoO$_{3−x}$ modification in suppressing electron injection, we then evaluate the DC bias stress stability of the devices with a constant V_{gs} and V_{ds}. **Figure 3** compares the stability performance of the FETs with unmodified and modified electrodes in the saturation operation regime. (Curves under 10 000 s DC bias stress can be found in Figure S3 (Supporting Information) for the OFET and GFET devices.)
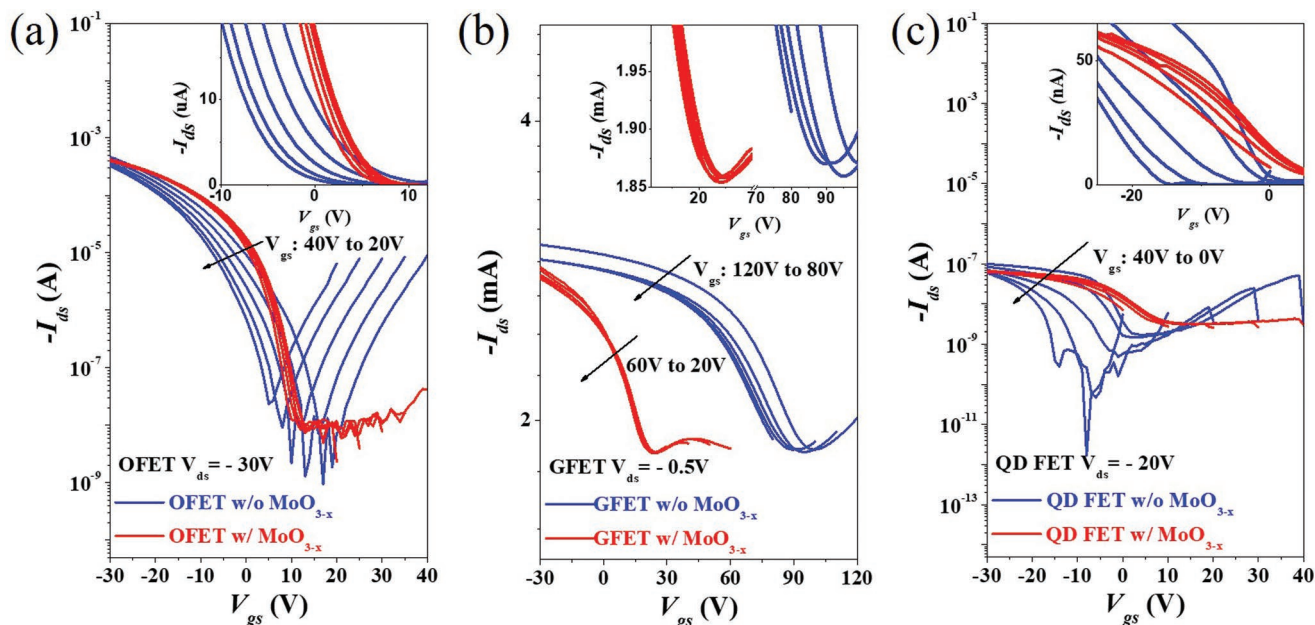

Figure 2. Transfer characteristics of the a) OFETs, b) GFETs, and c) QD FETs obtained with different scan ranges. (V_{gs} was always scanned from a positive bias to a negative bias, with different starting positive points and the same negative endpoint.) The curves of the devices with (w/ MoO$_{3−x}$) and without (w/o MoO$_{3−x}$) the MoO$_{3−x}$ modified electrodes are displayed in red and blue, respectively. The insets provide a zoom-in view of the transfer curves in a linear scale for better comparison of the threshold voltage shift.
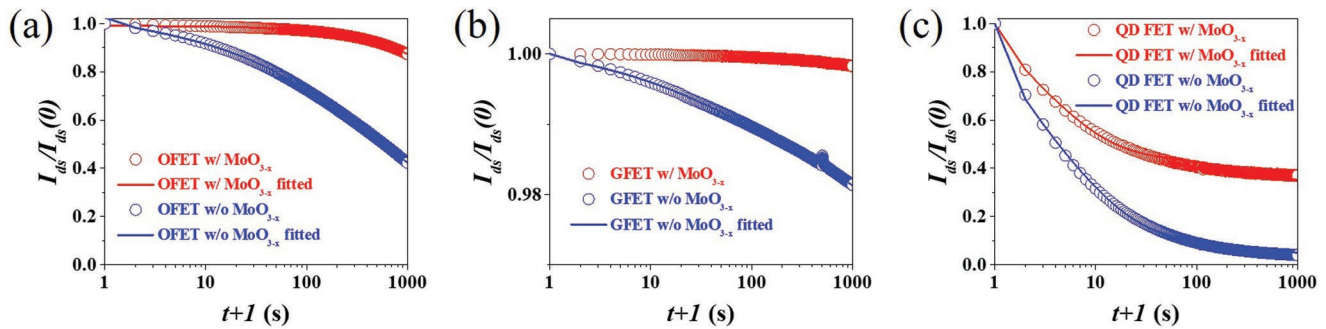
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Figure 3. Normalized source–drain current I_{ds} as a function of time t under DC bias stress with a constant V_{gs} and V_{ds} for a) OFETs ($V_{gs} = V_{ds} = -30$ V), b) GFETs ($V_{gs} = -20$ V, $V_{ds} = -0.5$ V), and c) QD FETs ($V_{gs} = -40$ V, $V_{ds} = -20$ V) with and without MoO_{3-x} modified electrodes. The data points were sampled at a 1 s interval, and the time axis is shifted by 1 s for log-scale display. The open circles represent the experimental data, and the solid lines represent the fitting results.

It can be seen that the OFET, GFET and QD FET devices all exhibit a much smaller current drop under bias stress after the MoO_{3-x} modification.

To understand these experimental results, it is important first to understand the differences in the physical processes occurring during the transfer scans and the bias stress measurements. In the transfer curve measurements, the gate bias was swept from a positive voltage to negative. In this process, a large number of electrons are first injected and trapped (when $V_{gs} > 0$), swiftly causing a positive V_{th} shift and thus an earlier turn-on of the transistor. On the other hand, in the bias stress measurements, the gate bias is kept at negative, and there will only be a small number of electrons "leaking" from the drain electrode into the semiconductor due to the lateral electric field, and they could reach the semiconductor/dielectric interface in the vicinity of the pinch-off region. Here the trapped electrons become localized ionized centers and could behave as hole Coulomb traps at the semiconductor/dielectric interface or the bulk semiconductor.[47–49] As a result, the mobility of holes will decrease, as shown in Figure S4 (Supporting Information), and the overall current will gradually decay. (We note that the electron trapping-induced bias-stress in ambient environments has also been associated with proton migration[19]; however, since our experiments for OFETs and QD FETs were conducted in a nitrogen-filled glove box we can exclude this mechanism.) Contact resistance is another possible reason for bias stress,[50] although it should not play a dominant role in long-channel FETs with a staggered structure. (Our devices have a top-contact bottom gate structure with > 50 µm channel length. A detail discussion about the contact resistance effect is provided in Supporting Information with Figures S5 and S6 (Supporting Information)).

We propose that the current decay in the bias stress measurement is caused by both the "trapped electron-induced hole traps" and "intrinsic hole traps" (i.e., defect states formed after FET fabrication). The DC stressing result provides direct evidence of the generality of the CSE approach in stability improvement, most likely via blocking of electron injection. The improvement appears to be more significant in the short time (0–100 s) window. We note that for the QD FETs the bias stress effect is still strong after the electrode modification. This suggests that hole trapping by the the the intrinsic defects of the QD film (e.g., QD surface defects) may occur in a very fast

timescale (within seconds, as reported previously[18]) and therefore also plays a significant role in the bias stress effect in the 100 s time window.

4. Double Trapping Processes and Bias Stress Mechanism

To further understand the dynamics of the bias stress and its relation with electron and hole trapping processes, we fit the bias-stress curves with stretched exponential functions that are commonly used to describe trapping induced current decay.[51] The fitting curves are also shown in Figure 3. (Note that we also used single exponential functions and their combinations[52,53] to fit the data but cannot obtain consistent fitting results for all FETs unless the unreasonable amount of exponential functions are used.) We found that using two stretched exponential functions, with one short time constant and one long time constant, can well fit all the bias stress data, suggesting that there are two types of trapping mechanisms that lead to the current decay. We hypothesize the two mechanisms are associated with a fast trapped electron-induced hole trapping process[47] and a slow "intrinsic" hole trapping (by the defect states originally existing in the FET) process, respectively. In the case of QD FET, the two mechanisms may occur at a similar timescale and collectively affect the device behavior; while for OFETs and GFETs trapped electron-induced hole trapping may play a predominant role in the short-time bias stress window. Here we assign the fast trapping process (i.e., the process happens within seconds to tens of seconds) to electron trapping due to the pronounced electron-injection induced threshold voltage shift observed in the fast transfer scans (Figure 2). More evidence for such an assignment is found through the analysis discussed below.

A double stretched exponential function is used for the fitting of the bias stress decay curves:

$$-I_{ds}(t) = I_0(\infty) + I_1 e^{-\left(\frac{t}{\tau_1}\right)^{\beta_1}} + I_2 e^{-\left(\frac{t}{\tau_2}\right)^{\beta_2}} \tag{1}$$

where $I_{ds}(t)$ is the source–drain current as a function of time t. $I_0(\infty)$ is the steady-state value and I_1, I_2 are the initial source/drain currents at $t = 0$ for the two trapping processes. And τ_1, τ_2 are the corresponding trapping lifetimes, whereas β_1, β_2 are the

Table 1. Fitting parameters based on the dual stretched exponential function for the DC bias stress results of the OFETs, GFETs, and QD FETs. The unit for $I_{ds}(0)$ is ampere and the unit for the time constant is second. In bold highlights that the weights of $I_1/I_{ds}(0)$ are greatly reduced by CSE.

Fitting parameters	$I_{ds}(0)$	$I_0/I_{ds}(0)$	$I_1/I_{ds}(0)$	τ_1	β_1	$I_2/I_{ds}(0)$	τ_2	β_2	r^2
OFET w/o MoO$_{3-x}$	-2.15×10^{-4}	0.0548	**0.0449**	68.4	1.000	0.9254	1206.3	0.434	0.9999
OFET w/ MoO$_{3-x}$	-7.35×10^{-4}	0.1798	**0.0022**	68.3	1.000	0.8086	9501.4	0.833	0.9997
GFET w/o MoO$_{3-x}$	-3.78×10^{-4}	0.0761	**0.0082**	33.5	0.606	0.9157	9 626 746.6	0.485	0.9985
GFET w/ MoO$_{3-x}$[a]	-3.56×10^{-3}	0.0572	–	–	–	0.9428	9 559 833.8	0.709	0.9943
QD FET w/o MoO$_{3-x}$	-6.12×10^{-8}	0.0003	**0.9341**	4.8	0.438	0.0857	1893.9	0.428	0.9972
QD FET w/ MoO$_{3-x}$	-1.18×10^{-8}	0.2690	**0.6200**	5.0	0.432	0.1221	9290.9	0.717	0.9959

[a]For GFET with MoO$_{3-x}$ modified electrode, the weight $I_1/I_{ds}(0)$ is less than 0.1%. Thus the related columns are left blank.

dispersion parameters of the barrier energy height for charge trapping.[54] The nonlinear least-squares method was used for the fitting, and following the method in ref. [55], we applied two steps to extract the long- and short-time components of the curves: in the first step we used the $t > 500$ s part of the curve for the fitting to extract the long-time constant τ_2 and its related β_2; and in the second step we used the full data range to fit the short-time constant τ_1 and its related β_1, while keeping τ_2 and β_2 fixed.

The fitting curves are plotted in Figure 2, and the fitting parameters are summarised as **Table 1**. We found that for both OFETs and QD FETs the MoO$_{3-x}$ electrode modification does not change τ_1 and β_1 much, but on the other hand drastically reduces the weighting factor, $I_1/I_{ds}(0)$ (highlighted in bold in Table 1). This result suggests that the function of MoO$_{3-x}$ is mainly reducing the number of trapping events, instead of changing the type of trapping. Relating the result with our previous observation that MoO$_{3-x}$ reduces electron injection, we can confirm that the short-time bias-stress decay is indeed dominated by electron trapping-induced hole trapping. For the long-time decay component, we find that the τ_2 and β_2 values extracted for the unmodified devices are significantly smaller as compared to those of the MoO$_{3-x}$ modified devices. This is probably because there exists a time window where the two trapping mechanisms (i.e., trapped electron-induced hole trapping process and "intrinsic" hole trapping) both occur and contribute significantly for the current decay. Note that β_2 is less than 0.5 for all unmodified devices, suggesting that there are multiple types of trapping events contributing to the long-time decay. After MoO$_{3-x}$ modification, β_2 is increased to the range of 0.7–0.85, indicating that in this case, the electron-trapping induced hole trapping has much less contribution in the long-time decay component. The time constant τ_2 is close to 10^4 s, and it may be close to reflecting the dynamic hole trapping processes induced by the intrinsic p-type defect states of the FETs. For the GFETs, the decay is very slow and almost disappears after MoO$_{3-x}$ modification, the trend of the bias stress reduction is the same as that of the OFET and QDFET devices, but it may become inaccurate to compare the fitting parameters due to the small variation in current. It is worth mentioning that the CSE approach could be applied to n-type FETs, especially if the bias stress effect is mainly associated with deep hole traps. For the n-type devices, other oxide material such as zinc oxide (ZnO) may be used as the hole blocking layer.[56]

5. Noise Performace with and without Charge Selective Electrode

The improved electrical stability should lead to reduced noise generation of the devices, and this is indeed observed in all the FETs with MoO$_{3-x}$ modified electrodes, as demonstrated in **Figure 4**. It is observed that the normalized noise spectral density curves of all the FETs exhibit the frequency dependence of $1/f$ noise, which is commonly found in organic, 2D and QD semiconductors with a considerable degree of energetic disorder.[12,14,57–59] The curves can be well fitted with the model $S = S_I/I_D^2 \propto 1/f^\alpha$ by using α close to 1. Here S is the normalized noise spectrum with unit of Hz^{-1}, S_I is the noise current spectrum density with unit of A^2 Hz^{-1}, I_D is the current measured in dark, and the unitless parameter α indicates the nature of noise, i.e., α close to 1 corresponding to $1/f$ noise and α close to 0 corresponding to white noise. (For quantitative comparison of the noise level, the calculated noise amplitudes $A = \frac{1}{N}\sum_{k=0}^{N} f_k S_k$ are listed in Table S2 (Supporting Information). We also compared the noise current with the shot noise in the high frequency range as shown in Figure S7 (Supporting Information)). As the $1/f$ noise is closely associated with charge trapping and
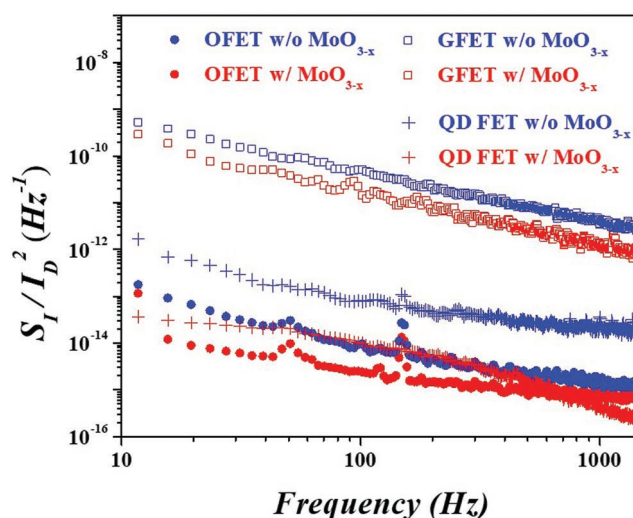

Figure 4. Normalized noise spectral density (S_I/I_D^2) as a function of frequency for the OFETs, GFETs, and QD FETs with and without MoO$_{3-x}$ modified electrodes. The peaks at near 50 Hz and its harmonics are due to the power supply interference.

de-trapping processes,[28,57] the MoO_{3-x} modification induced noise reduction indicates a suppression of these processes, consistent with the stability results obtained in Section 4. Our noise results are better than the reported noise level for light sensing based on organic phototransistor,[12] and QD phototransistor,[14] indicating the important application of CSE strategy in phototransistors. The normalized noise spectrum density of GFET is comparable with reported noise level.[57] The low-noise property is critical for applications such as detectors,[12,14] where the input (or sensing) signal is very small.

6. Conclusion

In conclusion, we demonstrated MoO_{3-x} based CSE as a general strategy to suppress electron injection-induced electrical instability in p-type OFETs, QD FETs, and GFETs. We show that the insertion of a thin MoO_{3-x} layer between the source-drain electrodes and the semiconductor can effectively suppress electron injection into the active layer of the FETs and thereby greatly reduce the $V_{th/Dirac}$ shift during transfer scans, improve the DC stability under bias stress, and decreases the low-frequency noise current of the devices. We have further analyzed the bias-stress dynamics and correlate the process with electron trapping and hole trapping, and the results suggest that electron trapping-induced hole trapping mainly accounts for the fast decay component of a bias stress process. The fabrication simplicity of the MoO_{3-x} based CSE and its great efficacy in stability improvement and noise reduction make the CSE a favorable device configuration to adopt in FETs for sensing/detection applications.

7. Experimental Section

Fabrication of Field-Effect Transistors: The heavily doped silicon wafers (working as gate electrodes) covered with 300 nm SiO_2 (working as the dielectrics with a capacitance density of 11.5 nF cm^{-2}) were used as the substrates. The substrates were ultrasonically cleaned by de-ionic (DI) water, acetone, and isopropyl alcohol (IPA) for 10 min, respectively. After dried by nitrogen flow, the substrates were treated with UV ozone plasma (Novascan UV Ozone Cleaners) for 30 min. For organic field-effect transistors (OFETs), the substrates were treated by gas OTS-8 (Sigma-Aldrich) overnight by putting the substrate in a vacuum chamber (<13 psi) with a small bottle (15 mL, open) of the OTS-8 pure solution. After the gas OTS-8 treatment, the substrates were ultrasonically cleaned by n-hexane (Sigma-Aldrich) for three times, three min per time, and dried by N_2 flow again. The polymer film was deposited via spin coating (1000 rpm, 60 s) using DPP-DTT (Ossila) solution (8 mg mL^{-1} in dichlorobenzene). And the film was thermally annealed at 135 °C for 20 min in N_2 glove box. For graphene field-effect transistors (GFETs), single layer graphene was grown by chemical vapor deposition (CVD) method as in Ref. [39] and transferred to cleaned substrates. For quantum dot field-effect transistors (QD FETs), the commercial PbS QD solution (25 mg mL^{-1} in toluene, Xingzi New Materials Technology Development Co., Ltd., OA-11 311 with emission band of 1050 ± 50 nm) was precipitated five times from solution in methanol and recast into hexane. Following a sixth crash-out, the QD precipitate was recast into octane to form solution (25 mg mL^{-1}, filtered by 45 μm filter membrane). The filtered solution was then spin-coated (1000 rpm, 60 s) in N_2 glove box onto cleaned substrates in the N_2 glove box. The as-formed film was then treated in a solution of 0.5% EDT in acetonitrile (by volume), and separately spun dried with the same spin-coating condition. Finally, the EDT-treated film was rinsed for 30 s in pure acetonitrile to remove the residual ligands. For all FETs, the drain/source electrodes (50 nm Au, or 15 nm MoO_3 (Sigma-Aldrich)/ 50 nm Au, W/L = 17 × 2.7 mm/ 60 μm for OFETs and QD FETs, W/L = 1.5 mm/100 μm for GFETs) were deposited via thermal evaporation with shadow masks.

Characterizations: The transfer characteristic and bias stress stability test were conducted by Keithley 2612 sourcemeter in dark condition (in N_2 glove box for OFETs and QD FETs, in the air for GFETs). The noise was measured by FFT spectrum analyzer SR760 with silver gel bonding devices powered by batteries ($V_{ds} = V_{gs} = -27$ V for OFETs; $V_{ds} = -1.5$ V, $V_{gs} = -27$ V for GFETs; $V_{ds} = -18$ V, $V_{gs} = -36$ V for QD FETs) in a metal EM shielding box after 5 min stressing in dark condition in the air (PSD in dBVrms, BMH window, AC coupling, average number 1000). The surface potential was recorded by Kelvin probe force microscopy (KPFM) method by Bruker Dimension 5000 Scanning Probe Microscope (SPM), where the gold film was deposited using peel-off method for the sample as in ref. [26].

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

[1] H. Sirringhaus, *Adv. Mater.* **2014**, *26*, 1319.
[2] Y. Yuan, G. Giri, A. L. Ayzner, A. P. Zoombelt, S. C. Mannsfeld, J. Chen, D. Nordlund, M. F. Toney, J. Huang, Z. Bao, *Nat. Commun.* **2014**, *5*, 3005.
[3] A. Perinot, P. Kshirsagar, M. A. Malvindi, P. P. Pompa, R. Fiammengo, M. Caironi, *Sci. Rep.* **2016**, *6*, 38941.
[4] Y. Xu, H. Sun, A. Liu, H. H. Zhu, W. Li, Y. F. Lin, Y. Y. Noh, *Adv. Mater.* **2018**, *30*, 1801830.
[5] H. Heo, M. H. Lee, J. Yang, H. S. Wee, J. Lim, D. Hahm, J. W. Yu, W. K. Bae, W. B. Lee, M. S. Kang, K. Char, *Nano Lett.* **2017**, *17*, 2433.
[6] F. Hetsch, N. Zhao, S. V. Kershaw, A. L. Rogach, *Mater. Today* **2013**, *16*, 312.
[7] M. Chhowalla, D. Jena, H. Zhang, *Nat. Rev. Mater.* **2016**, *1*, 16052.
[8] N. Dontschuk, A. Stacey, A. Tadich, K. J. Rietwyk, A. Schenk, M. T. Edmonds, O. Shimoni, C. I. Pakes, S. Prawer, J. Cervenka, *Nat. Commun.* **2015**, *6*, 6563.

[9] M. T. Hwang, Z. J. Wang, J. L. Ping, D. K. Ban, Z. C. Shiah, L. Antonschmidt, J. Lee, Y. S. Liu, A. G. Karkisaval, A. T. C. Johnson, C. H. Fan, G. Glinsky, R. Lal, *Adv. Mater.* **2018**, *30*, 1802440.

[10] F. Schwierz, *Nat. Nanotechnol.* **2010**, *5*, 487.

[11] T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, *Nat. Mater.* **2010**, *9*, 1015.

[12] H. Xu, J. Liu, J. Zhang, G. Zhou, N. Luo, N. Zhao, *Adv. Mater.* **2017**, *29*, 1700975.

[13] X. Wu, Y. Ma, G. Zhang, Y. Chu, J. Du, Y. Zhang, Z. Li, Y. Duan, Z. Fan, J. Huang, *Adv. Funct. Mater.* **2015**, *25*, 2138.

[14] M. Chen, H. Lu, N. M. Abdelazim, Y. Zhu, Z. Wang, W. Ren, S. V. Kershaw, A. L. Rogach, N. Zhao, *ACS Nano* **2017**, *11*, 5614.

[15] Y. Ohno, K. Maehashi, K. Matsumoto, *J. Am. Chem. Soc.* **2010**, *132*, 18012.

[16] H. Njoum, P. A. Kyriacou, *Sci. Rep.* **2017**, *7*, 1406.

[17] W. Liu, X. Sun, Z. Fang, Z. Wang, X. A. Tran, F. Wang, L. Wu, G. I. Ng, J. Zhang, J. Wei, *IEEE Electron Device Lett.* **2012**, *33*, 339.

[18] T. P. Osedach, N. Zhao, T. L. Andrew, P. R. Brown, D. D. Wanger, D. B. Strasfeld, L.-Y. Chang, M. G. Bawendi, V. Bulovic, *ACS Nano* **2012**, *6*, 3121.

[19] P. A. Bobbert, A. Sharma, S. G. Mathijssen, M. Kemerink, D. M. de Leeuw, *Adv. Mater.* **2012**, *24*, 1146.

[20] M. Nikolka, I. Nasrallah, B. Rose, M. K. Ravva, K. Broch, A. Sadhanala, D. Harkin, J. Charmet, M. Hurhangee, A. Brown, *Nat. Mater.* **2017**, *16*, 356.

[21] M. Nikolka, G. Schweicher, J. Armitage, I. Nasrallah, C. Jellett, Z. Guo, M. Hurhangee, A. Sadhanala, I. McCulloch, C. B. Nielsen, *Adv. Mater.* **2018**, *30*, 1801874.

[22] Y. Liu, J. Tolentino, M. Gibbs, R. Ihly, C. L. Perkins, Y. Liu, N. Crawford, J. C. Hemminger, M. Law, *Nano Lett.* **2013**, *13*, 1578.

[23] A. A. Sagade, D. Neumaier, D. Schall, M. Otto, A. Pesquera, A. Centeno, A. Z. Elorza, H. Kurz, *Nanoscale* **2015**, *7*, 3558.

[24] H. Phan, M. Wang, G. C. Bazan, T. Q. Nguyen, *Adv. Mater.* **2015**, *27*, 7004.

[25] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, R. H. Friend, *Nature* **2005**, *434*, 194.

[26] X. Wang, J. B. Xu, C. Wang, J. Du, W. Xie, *Adv. Mater.* **2011**, *23*, 2464.

[27] J. M. Luther, M. Law, Q. Song, C. L. Perkins, M. C. Beard, A. J. Nozik, *ACS Nano* **2008**, *2*, 271.

[28] H. Phan, M. J. Ford, A. T. Lill, M. Wang, G. C. Bazan, T. Q. Nguyen, *Adv. Funct. Mater.* **2017**, *27*, 1701358.

[29] D. K. Hwang, C. Fuentes-Hernandez, J. Kim, W. J. Potscavage Jr., S. J. Kim, B. Kippelen, *Adv. Mater.* **2011**, *23*, 1293.

[30] W. C. Shin, S. Seo, B. J. Cho, *Appl. Phys. Lett.* **2011**, *98*, 153505.

[31] J. Kettle, H. Waters, M. Horie, S. Chang, *J. Phys. D: Appl. Phys.* **2012**, *45*, 125102.

[32] C. Adachi, S. Tokito, T. Tsutsui, S. Saito, *Jpn. J. Appl. Phys.* **1988**, *27*, L713.

[33] C.-H. M. Chuang, P. R. Brown, V. Bulović, M. G. Bawendi, *Nat. Mater.* **2014**, *13*, 796.

[34] J. Bullock, M. Hettick, J. Geissbühler, A. J. Ong, T. Allen, C. M. Sutter-Fella, T. Chen, H. Ota, E. W. Schaler, S. De Wolf, *Nat. Energy* **2016**, *1*, 15031.

[35] D. Kumaki, Y. Fujisaki, S. Tokito, *Org. Electron.* **2013**, *14*, 475.

[36] T. Richards, H. Sirringhaus, *Appl. Phys. Lett.* **2008**, *92*, 023512.

[37] C.-H. Wang, X. Gao, Y.-N. Zhong, J. Liu, J.-L. Xu, S.-D. Wang, *Org. Electron.* **2017**, *42*, 367.

[38] J. Li, Y. Zhao, H. S. Tan, Y. Guo, C.-A. Di, G. Yu, Y. Liu, M. Lin, S. H. Lim, Y. Zhou, *Sci. Rep.* **2012**, *2*, 754.

[39] S. Zhou, Y. Su, Y. Xiao, N. Zhao, J. Xu, C. Wong, *Nanotechnology* **2014**, *25*, 265201.

[40] P. R. Brown, D. Kim, R. R. Lunt, N. Zhao, M. G. Bawendi, J. C. Grossman, V. Bulović, *ACS Nano* **2014**, *8*, 5863.

[41] Y. Zhou, C. Fuentes-Hernandez, J. Shim, J. Meyer, A. J. Giordano, H. Li, P. Winget, T. Papadopoulos, H. Cheun, J. Kim, *Science* **2012**, *336*, 327.

[42] M. C. Gwinner, R. D. Pietro, Y. Vaynzof, K. J. Greenberg, P. K. Ho, R. H. Friend, H. Sirringhaus, *Adv. Funct. Mater.* **2011**, *21*, 1432.

[43] C. Liu, Y. Xu, Y. Y. Noh, *Mater. Today* **2015**, *18*, 79.

[44] D. Natali, M. Caironi, *Adv. Mater.* **2012**, *24*, 1357.

[45] C. Liu, G. T. Li, R. Di Pietro, J. Huang, Y. Y. Noh, X. Y. Liu, T. Minari, *Phys. Rev. Appl.* **2017**, *8*, 034020.

[46] T. Okachi, T. Kashiki, K. Ohya, *Proc. SPIE* **2015**, *9568*, 95680I.

[47] M. F. Calhoun, C. Hsieh, V. Podzorov, *Phys. Rev. Lett.* **2007**, *98*, 096402.

[48] V. I. Arkhipov, E. V. Emelianova, P. Heremans, H. Bassler, *Phys. Rev. B* **2005**, *72*, 235202.

[49] A. Kadashchuk, V. I. Arkhipov, C. H. Kim, J. Shinar, D. W. Lee, Y. R. Hong, J. I. Jin, P. Heremans, H. Baessler, *Phys. Rev. B* **2007**, *76*, 12337.

[50] C. Liu, Y. Xu, Y. Li, W. Scheideler, T. Minari, *J. Phys. Chem. C* **2013**, *117*, 12337.

[51] G. Gu, M. G. Kane, J. E. Doty, A. H. Firester, *Appl. Phys. Lett.* **2005**, *87*, 243512.

[52] C.-C. Shih, Y.-S. Lee, K.-L. Fang, C.-H. Chen, F.-Y. Gan, *IEEE Trans. Device Mater. Reliab.* **2007**, *7*, 347.

[53] Y. J. Kim, Y. G. Lee, U. Jung, S. Lee, S. K. Lee, B. H. Lee, *Nanoscale* **2015**, *7*, 4013.

[54] H. H. Choi, M. S. Kang, M. Kim, H. Kim, J. H. Cho, K. Cho, *Adv. Funct. Mater.* **2013**, *23*, 690.

[55] G. Gu, M. G. Kane, *Appl. Phys. Lett.* **2008**, *92*, 33.

[56] T. Shirakawa, T. Umeda, Y. Hashimoto, A. Fujii, K. Yoshino, *J. Phys. D: Appl. Phys.* **2004**, *37*, 847.

[57] A. A. Balandin, *Nat. Nanotechnol.* **2013**, *8*, 549.

[58] Y. Lai, H. Li, D. K. Kim, B. T. Diroll, C. B. Murray, C. R. Kagan, *ACS Nano* **2014**, *8*, 9664.

[59] P. Necliudov, S. Rumyantsev, M. Shur, D. Gundlach, T. Jackson, *J. Appl. Phys.* **2000**, *88*, 5395.